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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,075	06/15/2001	Marc Donis	A00774/70178 (EJR)	1583
34705	7590	02/14/2006	EXAMINER	
			MOORE, IAN N	
			ART UNIT	PAPER NUMBER
			2661	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/883,075	DONIS ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Ian N. Moore	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 06 October 2005.  
 2a) This action is FINAL. 2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1,2,4-9,11-17 and 33-43 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,4-9,11-17 and 33-43 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### *Claim Objections*

1. Claim 6 is objected to because of the following informalities:

**Claim 6** recites, “**the** switch” in line 3. For clarity, it is suggested to change to “**a** switch”.

**Claim 14** recites, “a plurality of input ports that **receive** communicating units **from the switch to the network**” in line 2-3. It is unclear whether the communicating units are received from the switch, at the switch, or switch to the network.

Appropriate correction is required.

### First set of rejection

#### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-9, 11-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fan (US 6,324,165), as set forth in previous office action, and hereby incorporated.

**Second set of rejection**

3. Claims 1,2,6-9,11-17,33-37,42 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Caldara (US005872769A).

**Regarding Claims 1 and 9,** Caldara discloses a switch (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the switch comprising:

a plurality of ports (see FIG. 1, Input ports 0-n 20 and Output port 0-n 22);  
a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first queue depth (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold of first Input/output buffer/queue) coupled to one of the ports (see FIG. 1, couple to input/output ports) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second queue depth (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold of second Input/output buffer/queue) coupled to the one of the ports (see FIG. 1, couple to input/output ports) to store communication units corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and

Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, and to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to manage/adjust a depth of at least one of the first queue depth of the first buffer memory or the second queue depth of the second buffer memory (see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/depth).

**Regarding Claim 2**, Caldara discloses a sorter unit (see FIG. 1, a combined scheduling/sorting system of Switch Allocation Table (SAT) (see FIG. 3) and BA 12) coupled to the first buffer memory and the second buffer memory to selectively store a communication unit in the first buffer or the second buffer based on a quality of service level of the communication unit (see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67; the combined switching system schedules/sorts the ATM cells according to their service classes).

**Regarding Claim 6**, Caldara discloses means for determining performance characteristics of the switch (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12 determines performance of the switch 10; see col. 4, line 32-64).

**Regarding Claim 7**, Caldara discloses the first buffer memory and the second buffer memory are regions of memory in a contiguous random access memory device (see col. 5, line

65 to col. 6, line 4; each TSPP/ includes cell buffer RAM which are organized/contiguous into queues).

**Regarding Claims 8, 17 and 42,** Caldara discloses wherein the communication units are ATM cells (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells).

**Regarding Claim 11,** Caldara discloses a plurality of output ports (see FIG. 1, Output port 0-n) that output communication units from the switch to the network (see col. 5, line 35-50; output ports connects the switch 10 to ATM network); and

the first buffer memory and the second buffer memory (see FIG. 1-2, first and second Input queue 32 a-m) are coupled to one of the plurality of output ports (see FIG. 1, Output port 0-n), to store communication units to be output to the one of the plurality of output ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Input queues stores ATM cells to output to output ports).

**Regarding Claim 12,** Caldara discloses each of the plurality of output ports has a respective first buffer memory (see FIG. 1-2, first output queue 34 a) and a respective second buffer memory (see FIG. 1-2, second output queue 34 m) to store communication units transmitted across the respective output port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second output queues stores ATM cells which are transmitted to output port).

**Regarding Claim 13,** Caldara discloses each of the plurality of output ports has a respective buffer manager (see FIG. 1, a control in output port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second output queue 34 a and m) based on a corresponding quality of service level of

the communication units (see FIG. 6, storing in VBR or ABR output queues; see col. 8, line 65 to col. 9, line 40), and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second output queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

**Regarding Claim 14,** Caldara discloses a plurality of input ports (see FIG. 1, Input ports 0-n 20) that receive communication units from the switch to the network (see col. 5, line 35-50; input ports receives ATM cells the switch 10 to ATM network); and the first buffer memory (see FIG. 1-2, first output queue 34 a) and the second buffer memory (see FIG. 1-2, first output queue 34 m) are coupled to one of the plurality of input ports (see FIG. 1, Input ports 0-n 20), to store communication units received on the one of the plurality of input ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Output queues 34 stores ATM cells receives from input ports).

**Regarding Claim 15,** Caldara discloses each of the plurality of input ports (see FIG. 1, Input ports 0-n 20) has a respective first buffer memory (see FIG. 1-2, first Input queue 32 a) and a respective second buffer memory (see FIG. 1-2, second Input queue 32 m) to store communication units transmitted across the respective input port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second input queues stores ATM cells which are transmitted across input port).

**Regarding Claim 16,** Caldara discloses each of the plurality of input ports has a respective buffer manager (see FIG. 1, a control in input port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second

input queue 32 a and m) based on a corresponding quality of service level of the communication unit, and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second input queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

**Regarding Claims 33 and 43**, Caldara discloses a buffer element (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the buffer element comprising:

a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first depth (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold of first Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second depth (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold of second Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first

buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to adjust at least one of the first depth of the first buffer memory or the second depth of the second buffer memory (see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/depth), based on a total memory available to the buffer element (see FIG. 7, total bandwidth available (i.e. total of used & unused bandwidth threshold), the first and second depths (see FIG. 7, used bandwidth threshold by the queues), and the quality of service provided by each buffer memory (see col. 9, line 1-40; service quality of each queue); see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67.

**Regarding Claim 34**, Caldara discloses wherein the characteristic is selected from the group consisting the communication unit processing rate for one of the quality of service levels (see col. 6, line 30-40; see col. 14, line 21-27; switch utilization/processing rate for quality service classes) and the communication unit delay rate for one of the quality of service levels (see col. 1, line 27-50; see col. 2, line 64 to col. 3, line 6; see col. 7, line 40-46; see col. 9, line 21-40; see col. 13, line 33-40; delay bound/parameter/rate for service class priorities).

**Regarding Claims 35 and 36**, Caldara discloses each of the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores communication units for a single port wherein the single port is an output port (see FIG. 1 and 6, Output port 0) in a communication network switch (see FIG. 1,2,6; ATM switch 10); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

**Regarding Claims 37**, Caldara discloses wherein the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores the communication units for each port of a switch in the communication network (see FIG. 1 and 6, Input or Output port 0-n); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4,5,40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara in view of Holender (US006069894A).

**Regarding Claims 4 and 40**, Caldara discloses means for iteratively determining possible depth assignments to determine the first depth and the second depth (see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically determines each queue for dynamic threshold/depth).

Caldara does not explicitly disclose iteratively searching possible assignments. However, Holender teaches iteratively searching possible assignments to determine the optimal value in ATM network (see col. 5, line 42-46; see col. 13, line 39-60; col. 16, line 10 to col. 17, line 27; hill climbing process is used to search possible assignment/value to determine optimize threshold/value). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide hill climbing search process, as taught by Holender in the system of Caldara, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

**Regarding Claims 5 and 41,** the combined system of Caldara and Holender discloses all limitation as described above in claim 1. Holender further teaches means for performing a steepest ascent hill climbing search (see col. 5, line 42-46; see col. 13, line 39-60; col. 16, line 10 to col. 17, line 27; ascend or step hill climbing process is used to search possible assignment/value to determine optimize threshold/value). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide hill climbing search process, as taught by Holender in the system of Caldara, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

6. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara in view of Kakuma (US005555265A).

**Regarding Claim 38,** Caldara discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Caldara does not explicitly disclose level for dropped. However, Kakuma teaches determining a priority level for dropped communication units for each of the quality of service levels (see col. 5, line 33-67; determining discard priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining discard priority for each quality class, as taught by Kakuma in the system of Caldara, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

**Regarding Claim 39,** Caldara discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Caldara does not explicitly disclose delay for quality service level. However, Kakuma teaches determining a priority level for communication units delay for each of the quality of service levels (see col. 14, line 45-65; see col. 15, line 20-34; determining delay priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining delay priority for each quality class, as taught by Kakuma in the system of Caldara, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

*Response to Arguments*

7. Applicant's arguments filed 10-6-2005 have been fully considered but they are not persuasive.

**Regarding claims 1 and 9, the applicant argued that, “...In the rejection, examiner states that “Fan discloses...and control how many cells get stored in each buffer...” With this statement, the Examiner acknowledges a distinction between Fan and the claimed invention...the claimed invention deals with adjusting depths of the buffers themselves, that is, how many cells can be stored in each buffer” in page 8, paragraph 4.**

**In response to applicant's argument, the examiner respectfully disagrees with the argument and the applicant's assumption on the examiner statements.**

First, examiner statements of “control how many cells get stored in each buffer” does not mean that the examiner is acknowledging a distinction between Fan and the claim invention. One skilled in the art will clearly see and know that that each buffer or queue in the ATM switch has a depth, size, threshold, or bandwidth. ATM cells are stored in accordance with the depth, size, threshold, or bandwidth of each buffer/queue, and thus, the number of cells store in the buffer/queue directly correspond to the depth, size, threshold, or bandwidth. The larger depth, size, threshold, or bandwidth, the more cells can be stored. When controlling or adjusting the number of ATM cells store in the buffer/queue (i.e. how many cells get stored in each buffer), it is essentially and equally controlling or adjusting the depth, size, threshold, or bandwidth (e.g. how many cells can be stored in each buffer). Thus, examiner finds no distinction between Fan and the claimed invention, nor examiner has ever acknowledged such distinction thereof.

Moreover, the applicant argued “the claimed invention deals with depths of the buffers **themselves**” (emphasis added). Claim 1 recites, “a buffer manager...adjust at least one of the

first depth of the first buffer memory..." Thus, it is clear that the depth of the buffer are controlled/adjusted by a buffer manager, **not "themselves"** as argued by the applicant.

**The applicant argued that, "...the claimed invention deals with cell loss when cells arrives at a buffer that is full...by adjusting the size of buffer depths to handle additional cells for that buffer...assuring that buffers with higher quality of service levels loss fewer cells than those low quality of service levels..."** in page 8, last paragraph.

**In response to applicant's argument** that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **cell loss when cells arrives at a buffer that is full, to handle additional cells for that buffer...assuring that buffers with higher quality of service levels loss fewer cells than those low quality of service levels**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

**The applicant argued that, "...Fan discloses allocation cells to different buffers, rather than adjusting the size/depth of buffers...This suggest that the depths of the buffer in Fan remain static, while allocation of cells to those buffers are adjusted..."** in page 9, paragraph 2.

**In response to applicant's argument, the examiner respectfully disagrees with the argument.** Fan clearly discloses

**The basic principle is that each class queue is treated like a virtual source whose service rate is dynamically adjusted to reflect the unused bandwidth available at a bottleneck point in the switch.** Specifically, each class is serviced at its guaranteed minimum rate plus a dynamically adjusted fair share of any available unused bandwidth. Scheduling consists of computing the queue service rate and implementing the rate shaping function for all queues. An important feature of this approach to scheduling is that all queues are reduced to a generic set of queues, and the QoS perceived by the class is determined by the bandwidth

guaranteed for the class. The generic queues are assigned to classes by the CAC. (see col. 10, line 11-25).

**Thus, it is clear that each class queue's length/source/depth/size corresponds to a rate which is dynamically adjusted.**

Fan discloses:

**The closed-loop controller adjusts the rate  $E(n)$  such that the error  $\epsilon(n) = Q(n) - Q_{\text{sub.0}}$  decreases in absolute value. However, the dynamics of the aggregate input traffic  $R(n)$  may be faster than that of the closed-loop controller. The queue length,  $Q(n)$ , in the second stage may grow to a large value before the closed-loop controller can bring it close to the target value  $Q_{\text{sub.0}}$ . This is caused by connections which transmit at rates significantly larger than their minimum guaranteed rates  $M_{\text{sub.}i}$ . A large value of  $Q(n)$  can adversely affect the delay performance of connections which are transmitting at rates close to their minimum rates. Since the response time of the closed-loop controller may be too slow to prevent overload at the second stage of the scheduler, in the preferred embodiment a separate overload control mechanism is provided.**

**When the second stage buffer exceeds a certain shape threshold, a feedback shape signal is transmitted to the DRC scheduler. This shape signal causes the scheduler to shape all queues at their guaranteed minimum rates,  $M_{\text{sub.}i}$ , and stop distribution of unused bandwidth. This action provides a quick overload control mechanism allowing relief of congestion. See col. 12, line 29-55.**

**Thus, it is clear that each class queue's length/source/depth/size with is associated rate is shaped/adjusted/controlled by DRC.**

Fan discloses:

A closed-loop proportional-derivative controller is used to compute  $E$  based on observations of the aggregate virtual queue length at the OP bottleneck. When the OP channel utilization exceeds a value  $U_{\text{sub.0}}$  (.apprxeq.95%, see step S1110), **the controller adjusts the value of  $E$  so as to maintain the aggregate virtual queue length corresponding to the OP bottleneck close to a target value  $N_{\text{sub.0}}$ .** When the OP channel utilization lies below  $U_{\text{sub.0}}$ , the controller adjusts  $E$  so that utilization will be brought close to  $U_{\text{sub.2}}$ . see col. 20, line 67 to col. 21, line 7.

**Thus, it is clear the queue length is adjusted according to the utilization.**

**Response to previous similar arguments** as set forth in the previous office are hereby incorporated.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that Fan as set forth in the 102 rejection is proper.

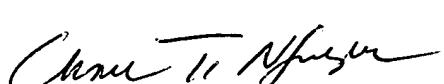
***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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CHAU NGUYEN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600